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PATENT APPLICATION FOR
METHOD FOR FABRICATING AN ISOLATED MICROELECTROMECHANICAL
SYSTEM (MEMS) DEVICE USING AN INTERNAL VOID

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CROSS-REFERENCE TO RELATED APPLICATIONS

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BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates to microelectromechanical systems (MEMS) and, in particular, relates to the fabrication of MEMS devices using an internal void.

2. Discussion of the Related Art

[0002] Microelectromechanical systems (MEMS) components are being progressively introduced into many electronic circuit as well as micro-sensor applications. Examples of MEMS components are electromechanical motors, radio frequency (RF) switches, high Q capacitors, pressure transducers and accelerometers. In one application, the MEMS device is an accelerometer having a movable component that, in response to an external stimulus, is actuated so as to vary the size of a capacitive air gap. Accordingly, the capacitance output of the MEMS device provides an indication of the strength of the acceleration.

[0003] When the MEMS device is an accelerometer, the device comprises a stationary MEMS element that is attached to a nonconductive substrate, and a movable MEMS element that has a substantial portion that is free from mechanical contact with the substrate that is therefore movable with respect to the stationary element.

[0004] One method of fabricating such components, often referred to as surface micro-machining, uses a sacrificial layer, such as silicon dioxide, that is deposited and bonded onto a substrate, such as single crystal silicon which has been covered with a layer of silicon nitride. A MEMS component material, for example polycrystalline silicon, is then deposited on the sacrificial layer, followed by a suitable conductor, such as aluminum, to form an electrical contact with the ambient environment. The silicon layer is then patterned by standard photolithographic techniques and then etched by a suitable reactive ion etching plasma or by wet chemistry to define the MEMS structure and to expose the

sacrificial layer, which may comprise silicon dioxide. The sacrificial layer is then etched to release the MEMS component.

[0005] Several disadvantages are associated with fabricating a MEMS device using a sacrificial layer. First, it requires the availability of an etching process that is capable of selectively etching the sacrificial layer without reacting with the other materials that will ultimately form the MEMS device. This limits the materials that may be used when fabricating the MEMS device. Additionally, the use of a sacrificial layer increases the amount of materials needed to form the MEMS device, thereby adding cost and complexity to the fabrication process. Furthermore, an additional etching step is needed to remove the sacrificial layer, thereby further reducing the efficiency of the fabrication process. In particular, because the structure forming the movable MEMS element is disposed on top of the sacrificial layer, a significant amount of time is needed to completely undercut the sacrificial layer. In fact, in some instances, holes are first etched through the base of the movable MEMS element in order to permit the etchant to access the sacrificial layer.

[0006] What is therefore needed is an improved method for manufacturing isolated MEMS devices using simplified etching processes that avoids the disadvantages associated with undercutting a sacrificial layer to release the movable MEMS element.

BRIEF SUMMARY OF THE INVENTION

[0007] The present inventors have recognized that an internal void may be formed while fabricating a MEMS device that facilitates the release of the movable MEMS element from the substrate while avoiding the difficulties associated with using a sacrificial layer.

[0008] In accordance with one aspect of the invention, a method for fabricating a MEMS device onto a substrate having a movable MEMS element portion free from the substrate and disposed adjacent a stationary MEMS element that is in mechanical communication with the substrate, comprises the steps of providing a wafer having opposed first and second surfaces, forming a recess into the first surface to produce a spacer member disposed at a periphery of the recess, mechanically connecting the spacer member to the substrate to form an internal void from the recess, wherein the void is further defined by the substrate, and removing a portion of the wafer into the void so as to release the movable MEMS element from the stationary MEMS element.

[0009] These and other aspects of the invention are not intended to define the scope of the invention for which purpose claims are provided. In the following description,

reference is made to the accompanying drawings, which form a part hereof, and in which there is shown by way of illustration, and not limitation, a preferred embodiment of the invention. Such embodiment does not define the scope of the invention and reference must be made therefore to the claims for this purpose.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] Reference is hereby made to the following figures in which like reference numerals correspond to like elements throughout, and in which:

[0011] Fig. 1 is a schematic sectional side elevation view of a MEMS device;

[0012] Fig. 2 is a sectional side elevation view of a wafer having a first and a second layer deposited thereon, and having photoresist deposited thereon and patterned, and usable to fabricate a MEMS device in accordance with a preferred embodiment;

[0013] Fig. 3 is a sectional side elevation view of the wafer illustrated in Fig. 2 after selectively etching the second layer and bonding the wafer to a substrate to form a composite structure and after depositing and patterning photoresist onto the composite structure;

[0014] Fig. 4A is a sectional side elevation view of the composite structure illustrated in Fig. 3 after selectively etching the wafer and removing the photoresist;

[0015] Fig. 4B is a sectional side elevation view of the composite structure illustrated in Fig. 4A after depositing and patterning additional photoresist;

[0016] Fig. 5 is a sectional side elevation view of a MEMS device formed after selectively etching the first layer of the composite structure illustrated in Fig. 4B and removing the photoresist;

[0017] Fig. 6 is a sectional side elevation view of a wafer, showing patterned photoresist, used to construct a MEMS device in accordance with an alternate embodiment of the invention;

[0018] Fig. 7 is a sectional side elevation view of the composite structure illustrated in Fig. 6 after selectively etching the wafer, removing the photoresist, and depositing a separating layer;

[0019] Fig. 8 is a sectional side elevation view of the wafer illustrated in Fig. 7 bonded to a substrate to form a composite structure;

[0020] Fig. 9 is a sectional side elevation view of the composite structure illustrated in Fig 8 after further selectively etching the wafer;

[0021] Fig. 10 is sectional side elevation view of a MEMS device formed after selectively etching the separating layer of the composite structure illustrated in Fig. 9;

[0022] Fig. 11 is a sectional side elevation view of a wafer having a first separating layer deposited thereon, and having photoresist deposited and patterned thereon, and used to construct a MEMS device in accordance with another alternate embodiment;

[0023] Fig. 12 is a sectional side elevation view of the wafer illustrated in Fig. 11 after selectively etching the first separating layer, removing the photoresist, and depositing a second separating layer thereon;

[0024] Fig. 13 is a sectional side elevation view of the wafer illustrated in Fig. 12 bonded to a substrate to form a composite structure; and

[0025] Fig. 14 is a sectional side elevation view of a MEMS device after selectively etching the wafer and the second separating layer of the composite structure illustrated in Fig. 13.

DETAILED DESCRIPTION OF THE INVENTION

[0026] Referring initially to Fig. 1, a schematic illustration of a MEMS device 10 includes a stationary MEMS element 12, which comprises a pair of stationary outer conductive members 13 extending upwardly from a substrate 14. The substrate 14 may be either conducting or insulating, depending on the intended application, and may comprise glass, high resistivity silicon, crystalline sapphire, crystalline silicon, polycrystalline silicon, silicon carbide, or ceramic such as alumina, aluminum nitride, and the like, or gallium arsenide. In fact, the substrate may comprise any material whatsoever that is suitable for supporting a MEMS device. An inner movable MEMS element 16 is disposed between the pair of stationary members 13, and includes a base layer 17 supporting two pairs of separated conductive elements 18 that extend upwardly from the base. It should be appreciated by those having ordinary skill in the art that movable MEMS element 16 is a beam that is supported at its distal ends by, for example, the substrate such that the middle portion of element 16 is free and movable relative to the stationary members 13. The outer two elements 13 are separated from moveable MEMS element 16 by a variable size gap 19, which could be the gap between the adjacent plates of a detection capacitor, as will become more apparent from the description below.

[0027] The MEMS device 10 could therefore perform any function suitable for a MEMS application. For example, the device could comprise an accelerometer whose movable MEMS element 16 is a beam that deflects in response to the external stimulus, such as an

acceleration or vibration of the device 10. Accordingly, as the size of the gaps 19 vary, so will the output capacitance, thereby providing a measurement of the amount of deflection of the movable MEMS element 16. A measurement of the amount of acceleration may thereby be obtained by measuring the capacitance of the device. The device 10 constructed in accordance with the present invention could further incorporate a wafer level cap and electrical traces connected to the stationary members 13, as described in "Method for Fabricating an Insolated Microelectromechanical System (MEMS) Device Incorporating a Wafer Level Cap" filed on even date herewith, the disclosure of which is hereby incorporated by reference.

[0028] If base layer 17 is formed utilizing an insulating material, as is the case in accordance with the preferred embodiment, the conductive elements 18 become electrically isolated from each other, thereby minimizing the risk that an electrical input will conduct across the device 10, which would jeopardize those elements disposed downstream of the MEMS output.

[0029] The MEMS device 10 may be fabricated in accordance with several embodiments that utilize an internal void to release the movable MEMS element 16 from the substrate 14 and stationary elements 13, as will now be described.

[0030] In particular, referring now to Fig. 2, a wafer 20, which is conducting and comprises silicon in accordance with the preferred embodiment, includes a first layer 24 deposited onto the upper surface 22 thereof. The first layer 24 is insulating in accordance with the preferred embodiment, and comprises silicon oxide (SiO_2). The oxide layer 24 may be formed by thermal oxidization of the wafer 20, or by depositing a layer of silicon dioxide, for example by using chemical vapor deposition (CVD) or plasma enhanced chemical vapor deposition (PECVD), as is understood by those having ordinary skill in the art.

[0031] Alternatively, the combination of wafer 20 and first insulating layer 24 could be realized using a silicon-on-insulator (SOI) wafer, in which the insulating layer would comprise silicon dioxide that is deposited onto the top surface of the SOI wafer 20 as commercially available. SOI wafers are commercially available having various thicknesses, and are thus selected in anticipation of the height of the final MEMS device. A method of etching a SOI wafer is described in a patent application filed on even date herewith and entitled "Method for Fabricating a Microelectromechanical System (MEMS) Device Using a Pre-patterned Substrate" the disclosure of which is hereby incorporated by reference.

the outer ends of the upper surface 25 of layer 24, defining a recess 30 therebetween whose base is further defined by upper surface 25.

[0036] Next, referring to Fig. 3, the remaining photoresist 28 is removed to expose the spacers 29, whose upper surface 27 is bonded to the upper surface 33 of the substrate 14 using a high temperature fusion bonding or any equivalent process as understood by those having ordinary skill in the art. Accordingly, an internal void is formed from the recess 30 that is further defined by the upper surface 33. The height D_3 of the spacer member 29 defines the height of the void 30, which should be sufficiently great to allow the release of the inner movable MEMS element 16 without the need to undercut a sacrificial layer that would be disposed beneath the movable MEMS element in accordance with conventional fabrication processes.

[0037] Wafer 20 may next be thinned to the desired thickness of the final MEMS device. If the wafer 20 is an SOI wafer, where the top silicon layer has been pre-selected to have the correct thickness for the MEMS device, the back silicon portion is largely removed by a grind and polish step, with the remaining portion, up to the silicon dioxide layer, removed by a chemical etch, such as TMAH. Next the silicon dioxide layer is removed in an HF etch. The silicon that remains would then have the desired thickness of the final MEMS device. If the original wafer 20 is a solid silicon wafer, then it must be carefully thinned to the desired thickness by a combination of physical grinding and polishing steps and chemical etching steps, taking care to maintain a uniform thickness across the entirety of the wafer.

[0038] Still referring to Fig. 3, photoresist members are now formed on the exposed surface of the silicon wafer 20 by depositing the photoresist and patterning with standard photolithographic techniques. In particular, a pair of outer photoresist members 34 are formed at the outer ends of the silicon wafer 20 and aligned with the spacers 29 to ultimately form the stationary outer MEMS element, as will become more apparent from the description below. A pair of middle photoresist members 36 are formed inwardly of outer pair 34 by a distance D_2 that will ultimately define a variable size gap disposed between the fabricated inner movable MEMS element and the stationary MEMS element. An inner pair of photoresist members 38 is formed on the wafer 20, and spaced inwardly therefrom, such that the silicon disposed beneath photoresist 36 and 38 will ultimately define conductive structures on the movable MEMS element.

[0039] With the photoresist 34, 36, and 38 in place, the silicon wafer 20 is anisotropically dry etched in an inductively coupled plasma (ICP), as is understood by those having

ordinary skill in the art. This etching process removes all silicon not disposed directly beneath one of the photoresist members to expose that portion of silicon dioxide layer 24 that is aligned with the etched silicon. The photoresist 34, 36, and 38 is then removed to reveal the inner and outer pairs of conductive elements 18 that extend upwardly from the silicon dioxide layer 24, as shown in Fig. 4A. Because the conductive elements 18 are aligned with the internal void 30, they will form part of the fabricated inner movable MEMS element 16. A third pair of oppositely disposed conductive elements 13 are formed, and are aligned with and are connected to the remaining spacers 29. Elements 13 are thus also connected to substrate 14 and will form part of the stationary conductive members 13 of the stationary MEMS element 12, as will now be described. At this point, the portion of conductive elements 18 that is disposed sufficiently inward of the distal end is only mechanically connected to stationary conductive members 13 via the silicon dioxide layer 24, it being appreciated that the elements are connected to the substrate 14 at their distal ends. Such an arrangement is described, for example in a patent application filed on March 13, 2001 and entitled "Microelectricalmechanical System (MEMS) Electrical Isolator with Reduced Sensitivity to Internal Noise" the disclosure of which is hereby incorporated by reference.

[0040] Referring now to Fig. 4B, photoresist 46 is deposited onto the structure and photolithographically patterned so as to protect that portion of the silicon dioxide layer 24 that is exposed between the conductive elements 18.

[0041] Accordingly, referring also to Fig. 5, only the silicon dioxide that is disposed between conductive elements 18 and 13, where it is not protected by the photoresist, is removed by applying to the exposed silicon dioxide an anisotropic etching plasma, such as trifluoro-methane (CHF_3), commercially known as fluoroform. The photoresist 46 is subsequently removed. Because the etched silicon dioxide is aligned with the internal void 30, and the layer 24 is etched into the void 30, the inner movable MEMS element 16 is released from the stationary element 12. In particular, the inner movable MEMS element 16 comprises the plurality of the conductive elements 18 that are spaced from each other, and connected via the insulating silicon dioxide base 17 to provide electrical isolation for the device 12. The outermost conductive elements 18, comprising the silicon 20, silicon dioxide 24, and silicon nitride or polycrystalline silicon 29 layers, are separated from the corresponding stationary conductive elements 13 via the variable size gap 19 so as to output an electrical signal whose strength is dependent on the size of the gap in response to movement by the inner MEMS element 16.

[0042] It should be appreciated that the primary purpose of insulating layer 24 is to form the top of the internal void 30 and, subsequently, the base 17 of the inner movable MEMS element 16. Accordingly, it need not be present on the outer sections of the wafer 20 adjacent the middle section in accordance with the preferred embodiment, but is deposited onto the entire wafer 20 for ease of deposition. In this regard, however, it should be appreciated that the outer conductive members 13 need not include the insulating layer 24.

[0043] Referring now to Fig. 6, a method of manufacturing the MEMS device 10 in accordance with an alternate embodiment begins with a wafer 48, which preferably comprises silicon, or an SOI wafer, as described above. A pair of outer photoresist members 52 is formed on the upper surface 50 of the wafer 48, and the wafer is subsequently anisotropically dry etched in an inductively coupled plasma (ICP). It should be appreciated that the width of each photoresist member 52 will define the corresponding width of the spacers, and consequently the width of the fabricated stationary conductive MEMS elements 13, as will become more apparent from the description below.

[0044] The middle portion of wafer 48 is partially etched for a predetermined amount of time sufficient to produce an outer pair of spacers 55 having a recess 54 therebetween of a depth D_4 (shown in Fig. 7). The etchant and photoresist 52 are subsequently removed once the recess 54 has achieved a sufficient depth. Depth D_4 should be sufficiently large to produce an internal void once the wafer is bonded to the substrate 14, and to enable the movable MEMS element 16 to be subsequently released from the substrate 48, as will be described in more detail below. It should be appreciated that the thickness of the final MEMS structure is the original thickness of the SOI wafer minus D_4 . Accordingly, D_4 is controlled to determine the final thickness of the fabricated MEMS device 10 and, accordingly, the magnitude of the resulting electrical signal.

[0045] Referring now to Fig. 7, layer 56, which is insulating in accordance with the preferred embodiment, is applied to the upper surface 50 of the wafer. The insulating properties of layer 56 will provide the electrical isolation for the fabricated MEMS device 10. The layer 56 preferably comprises silicon dioxide, but could alternatively comprise a selectively etchable material having suitable properties, such as silicon nitride, for example. The layer 56 may be formed using a standard oxidation process in which the wafer 48 is exposed to elevated temperatures in an oxygen atmosphere for a predetermined period of time. Alternatively, the layer 56 may be deposited using

chemical vapor deposition or plasma enhanced chemical vapor deposition, which would be preferable if it is desirable to reduce the temperatures experienced by the wafer 48. It is appreciated that the layer 56 is continuous where in alignment with the recess, as this portion of the layer will ultimately define the base 17 of the inner movable MEMS element 16.

[0046] In accordance with the illustrated embodiment, the spacers 55 comprise the portion of the unetched silicon at the outer ends of the wafer 48. The layer 56 may not provide a useful function for the spacers 55 if the substrate 14, shown in Fig. 8, is an insulator. It should therefore be understood that the spacers 55 need not include the insulating layer 56 formed thereon to provide the recess 54 in accordance with the preferred embodiment. If the substrate is a conductor, however, then the insulating properties associated with layer 56 may be necessary to provide electrical isolation for the device 10. For the purposes of clarity and convenience, spacers 55, as used herein, will include layer 56 throughout this description, it being appreciated that layer 56 need not form part of spacers 55 as described above.

[0047] Referring to Fig. 8, the upper surfaces 58 of spacers 55 are bonded to the upper surface 60 of substrate 14 using a high temperature fusion bonding, or any equivalent process, as described above. Accordingly, the recess 54 becomes an internal void that is further defined by the upper surface 60 of the substrate 14. Additionally, the portion of the wafer 48 that is aligned with the portion of layer ~~54~~⁵⁶ that is bonded to the substrate 14 will ultimately comprise the stationary outer conductive elements 13, as will now be described. RDA 4/14/01

[0048] Wafer 48 is then thinned to the desired thickness of the final MEMS device 10. If the wafer 48 is an SOI wafer, where the top silicon layer is the correct thickness for the MEMS device, the back silicon portion is largely removed by a grind and polish step, with the remaining portion, up to the silicon dioxide layer, removed by a chemical etch, such as TMAH. Next the silicon dioxide layer is removed in an HF etch. The remaining silicon is now the desired thickness of the final MEMS device. If the original wafer 48 is a solid silicon wafer, then it must be carefully thinned to the desired thickness by a combination of physical grinding and polishing steps and chemical etching steps, taking care to maintain a uniform thickness across the entirety of the wafer.

[0049] Next, referring to Fig. 9, photoresist is applied and patterned to the silicon wafer 48, which is then anisotropically etched down to the separating layer 56, as described above with reference to Figs. 3 and 4A. Accordingly, a pair of outer conductive elements

13 are formed along with inner conductive elements 18, which are supported by separating layer 56. As described above, conductive elements 18 and separator 56 will ultimately define the base of inner movable MEMS element 16. The outer conductive elements 18 are separated from the outer pair of inner conductive elements by a variable size gap 19. The final step in the fabrication process is to form the inner movable MEMS element 16. In particular, photoresist is applied and patterned so as to remain on that portion of layer 56 that is disposed between the conductive elements 18 and to expose only that portion of the layer that is aligned with the variable size gap 19.

[0050] Referring now to Fig. 10, the structure is processed for a sufficient amount of time to anisotropically etch all of the material comprising the exposed portion of layer 56, thereby releasing the inner movable MEMS element 16 from the stationary element 12. In particular, the inner movable MEMS element 16 comprises the plurality of the conductive elements 18 spaced apart from one another, and connected via the insulating silicon dioxide base 17 to provide electrical isolation in accordance with the preferred embodiment. The outermost conductive elements 18, comprising the silicon 48 and silicon dioxide 56, are separated from the corresponding stationary conductive elements 13 via the variable size gap 19 so as to output an electrical signal whose strength is dependent on the size of the gap in response to movement by the inner MEMS element 16.

[0051] Referring now to Fig. 11, a method of manufacturing the MEMS device 10 in accordance with an alternate embodiment is presented that avoids the difficulties associated with partially etching the silicon material. In particular, a silicon wafer 64 has deposited thereon a first layer 66, which may or may not be insulating. In accordance with the preferred embodiment, the layer comprises silicon dioxide because it is easily selectively etchable, it being appreciated that layer 66 could alternatively comprise any other selectively etchable material, such as silicon nitride. The thickness D_5 of layer 66 will define the depth of the corresponding internal void, and should be sufficiently deep so as to facilitate the release of the inner movable MEMS element from the substrate. Photoresist members 68 are formed on the outer ends of the upper surface 70 of layer 66 whose width will, as described above, correspond to the width of the fabricated spacers.

[0052] Referring now to Fig. 12, layer 66 is isotropically etched, and the photoresist 68 is removed, to reveal an outer pair of spacers 67 defining a recess 72 therebetween. Next, a second layer 74, which in the preferred embodiment comprises an insulator such as silicon dioxide, is deposited onto the wafer 64 and spacers 67. As described above,

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however, it should be appreciated that the spacers do not necessarily need to include the layer 74 that is disposed thereon unless layer 74 is needed to achieve electrical isolation.

[0053] It should be appreciated that while both layers 66 and 74 are formed from the same material in accordance with this embodiment, such an arrangement is feasible because the layers are not selectively etched with respect to one another. Rather, both layers 66 and 74 will be selectively etched with respect to the silicon wafer 64, as will be described in more detail below.

[0054] Referring now to Figs 13 and 14, the upper surfaces 69 of spacers 67 are bonded to the upper surface of the insulating substrate 14. Next, as described above with reference to Figs. 9 and 10, the wafer 64 is thinned, patterned, and etched to produce the outer stationary conductive elements 13 and inner movable conductive elements 18. Finally, the portion of the layer 74 that is aligned with the variable size gap 19 is etched to release the inner movable MEMS element 16 from the stationary element 12.

[0055] The above has been described as preferred embodiments of the present invention. It will occur to those that practice the art that many modifications may be made without departing from the spirit and scope of the invention. For example, it is appreciated by one having ordinary skill in the art that the structure of the inner movable MEMS element 16 may differ so long as it is electrically isolated and includes a conductive member that is operable to create a capacitance that varies according to. Accordingly, variations of the embodiments described herein will become apparent to those having ordinary skill in the art, and such variations are within the scope of the present invention, as defined by the following claims.